

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

After entry of the foregoing amendment, Claims 1-11 are pending in the present application. Claim 1 is amended, without introduction of new matter, by the present amendment.

In the outstanding Office Action, Claims 8 and 11 were rejected under 35 U.S.C. 112, second paragraph; Claims 1-4, 8, and 11 were rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,518,833 to Narendra et al. (hereinafter "Narendra"); Claims 1 and 5 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 6,771,117 to Nakai; and Claims 6, 7, 9, and 10 were indicated as allowable if rewritten to include all limitations of their base claim and intervening claims.

Applicant and Applicant's representatives thank Examiner Cunningham for the courtesy of the interview conducted January 19, 2005. During the interview, an agreement was reached that the independent claims would overcome Narendra if amended to recite the first transistor as having a variable resistance. The present response does not amend Claim 1 to recite the first resistor as having a variable resistance, but rather presents a new amendment and arguments believed to distinguish over Narendra (discussed *infra*).

Regarding the rejection of Claims 8 and 11 under 35 U.S.C. 112, second paragraph, Applicants note that Claims 8 and 11 read on at least Figure 8 of the present application; and that the claimed seventh transistor reads on element M8. Non-limiting examples of the first constant current generating part (Isw, M1, M2), first transistor (M3), second transistor (M4), seventh transistor (M8), eighth transistor (M9), ninth transistor (M10), and fourth current mirror (M4 and M8) are illustrated, as well. Accordingly, in view of the above explanation,

Applicants respectfully request that the rejection of Claims 8 and 11 under 35 U.S.C. 112, second paragraph, be withdrawn.<sup>1</sup>

Turning now to the rejection of Claims 1-4, 8, and 11 under 35 U.S.C. 102 as anticipated by Narendra, that rejection is respectfully traversed.

Amended Claim 1 recites that the voltage signal is input to the control electrode of the first transistor “from an exterior of the bias voltage generating circuit.”<sup>2</sup>

The outstanding Office Action cites the middle transistor 106 of Narendra as teaching the claimed first transistor. A voltage signal is not input to the control electrode (gate) of the middle transistor 106 from an exterior of Narendra’s voltage reference circuit. Rather, the voltage of the gate and drain of the middle transistor 102, which is arranged inside the voltage reference circuit, is input to the control electrode (gate) of the middle transistor 106. Thus, the middle transistor 106 does not teach the claimed first transistor.

Further, Narendra’s voltage reference circuit generates a reference voltage  $V_a$  which is “not flexible” and is “insensitive of linear temperature variation.”<sup>3</sup> In contrast, Claim 1 recites “a potential at said second current electrode of said second transistor functions as a first bias voltage.” A non-limiting example of the claimed bias voltage, with reference to Applicant’s Figure 1, is described as follows:

Thus, in the differential amplifier circuit in Fig. 1, even if the common mode voltage of the reference voltage signal  $V_{ref}$  decreases and the current flowing through the Nch MOS transistor NT3n decreases, the bias voltage to the Nch MOS transistor NT3n rises and thus the current flowing through the

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<sup>1</sup> For the Examiner’s convenience, Applicants note that non-limiting examples of the first constant current generating part of Claim 1 is illustrated by the circuitry (Isw, M1 and M2) in Figures 2, 5, 6 and 8; and by the circuitry (Isw, M1, M2, M4 and M8) in Figures 4 and 7. Non-limiting examples of the first transistor are illustrated by the transistor M3 in Figures 2, 5, 6, and 8; and by the transistor M9 in Figures 4 and 7. Non-limiting examples of the first current mirror circuit (M1 and M2), second current mirror circuit (M1 and M5), and third current mirror circuit (M7 and M8) of Claims 5 and 6 are illustrated in Figures 5 and 6. Non-limiting examples of the first current mirror circuit (M1 and M2) and second current mirror circuit (M4 and M8) of Claim 3 are illustrated in Figures 4 and 7.

<sup>2</sup> For support, see Figures 1-8. The reference voltage signal  $V_{ref}$  is not generated by the interior of the bias voltage generating circuit (in the differential amplifier circuit) in Figures 1 and 3; or the interior of the bias voltage generating circuit in Figures 2 and 4-8.

<sup>3</sup> Narendra, col. 4, line 18.

Nch MOS transistor NT3n increases, and the bias voltage generating circuit in Fig. 2 has a feedback action ensuring a constant current value through the Nch MOS transistor NT3n which is a constant current circuit.<sup>4</sup>

Thus, the bias voltage varies depending on the voltage signal input from the exterior of the bias voltage generating circuit, while Narendra's reference voltage Va is "not flexible."

In sum, Narendra does not teach (i) a voltage signal input "from the exterior of the bias voltage generating circuit;" or (ii) a bias voltage which varies depending on the voltage signal input from the exterior of the bias voltage generating circuit. Accordingly, Applicant respectfully requests that the rejection of Claims 1-4, 8, and 11 under 35 U.S.C. 102 as anticipated by Narendra be withdrawn.

Turning now to the rejection of Claims 1 and 5 under 35 U.S.C. 103 as unpatentable over Nakai, that rejection is respectfully traversed.

The Office Action cites Nakai, after modification to replace resistors R7 and R8 with resistor-connected NMOS transistors, as teaching each feature of Claim 1. However, as noted above, the voltage signal of Claim 1 is input to the control electrode of the first transistor "from the exterior of the bias voltage generating circuit." The substitution of a resistor-connected NMOS transistors for Nakai's resistors R7 and R8 would not inherently (necessarily) produce the claimed feature of a voltage signal input to the control electrode of the first transistor from an exterior of the bias voltage generating circuit. Thus, Nakai does not teach the claimed first transistor. Applicants also note that inputting a voltage signal to the control electrode (gate) of the claimed first transistor permits the resistance between the source and drain thereof to be varied. Nakai, on the other hand, teaches a fixed resistance for resistors R7 and R8.

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<sup>4</sup> Specification, page 12, line 12 to page 13, line 3.

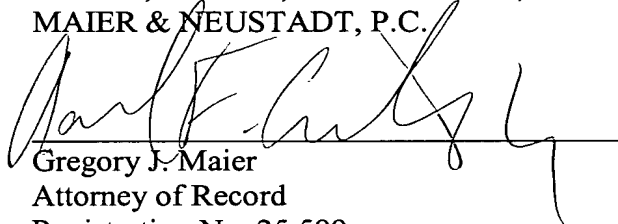
Accordingly, for the above stated reasons, Applicant respectfully requests that the rejection of Claims 1-4, 8, and 11 under 35 U.S.C. 103 as unpatentable over Nakai be withdrawn.

Accordingly, Applicant respectfully requests that the rejection of Claims 1 and 5 under 35 U.S.C. 103(a) as unpatentable over Nakai be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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